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### 1 [Translating between itanium and sparc memory consistency models](#)

[Lisa Higham, Lillian Jackson](#)

 July 2006 **SPAA '06**: Proceedings of the eighteenth annual ACM symposium on algorithms and architectures

**Publisher:** ACM [Request Permissions](#)

 Full text available: [Pdf](#) (258.74 KB)

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**Bibliometrics:** Downloads (6 Weeks): 3, Downloads (12 Months): 36, Citation

Our general goal is to port programs from one multiprocessor architecture ensuring that each program's semantics remains unchanged. This paper addresses the problem by determining the relationships between memory consistency

**Keywords:** itanium, memory consistency models, multiprocessors, porting, sparc

### 2 [Speculation techniques for improving load related instruction scheduling](#)

[Adi Yoaz, Mattan Erez, Ronny Ronen, Stephan Jourdan](#)

 May 1999 **ISCA '99**: Proceedings of the 26th annual international symposium on computer architecture

**Publisher:** ACM

 Full text available: [Publisher Site](#), [Pdf](#) (164.15 KB) Additional Information: [full citation](#), [abstract](#), [index terms](#)
**Bibliometrics:** Downloads (6 Weeks): 5, Downloads (12 Months): 42, Citation

State of the art microprocessors achieve high performance by executing instructions in an out-of-order engine. In an out-of-order engine, the instruction scheduler is responsible for scheduling instructions to execution units based on dependencies, latencies, ...

Also published in:

 May 1999 **SIGARCH Computer Architecture News** Volume 27 Issue 2

### 3 [Looking at History to Filter Allocations in Prediction Tables](#)

[Enric Moráncho, José María Llabería, Ángel Olivé](#)

 October 1999 **PACT '99**: Proceedings of the 1999 International Conference on Parallel Architectures and Compilation Techniques

**Publisher:** IEEE Computer Society

 Full text available: [Publisher Site](#)

 Additional Information: [full citation](#), [abstract](#)

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Dependencies between instructions impose an execution order that must guarantee the semantic correctness of programs. Recent works propose techniques to speculatively execute dependent operations, showing a significant improvement in performance.

**Keywords:** Address Prediction, Dynamic Classifications, Area Cost, Register File

#### 4 [The myth and realities of C.A.S.E. for documentation](#)

 [D. Patterson](#)

November 1989 **SIGDOC '89:** Proceedings of the 7th annual international conference on documentation

**Publisher:** ACM  [Request Permissions](#)

Additional Information: [full citation](#), [abstract](#), [index terms](#)

**Bibliometrics:** Downloads (6 Weeks): n/a, Downloads (12 Months): n/a, Citations: n/a

Hypertext seems to be the major focus of user documentation groups, and of documentation people. But system developers, engineers and architects are not. More of our documentation work will be coming from or going into ...

#### 5 [Reducing Design Complexity of the Load/Store Queue](#)

[Il Park](#), [Chong Liang Ooi](#), [T. N. Vijaykumar](#)

December 2003 **MICRO 36:** Proceedings of the 36th annual IEEE/ACM International Symposium on Microarchitecture


**Publisher:** IEEE Computer Society

Full text available:  Pdf (174.73 KB) Additional Information: [full citation](#), [abstract](#), [references](#)

**Bibliometrics:** Downloads (6 Weeks): 9, Downloads (12 Months): 42, Citations: 1

With faster CPU clocks and wider pipelines, all relevant microarchitectures must be scaled accordingly. There have been many proposals for scaling the issue queue hierarchy. However, nothing has been done for scaling the load/store queue.

#### 6 [Instruction set synthesis with efficient instruction encoding for configurable processors](#)

 [Jong-Eun Lee](#), [Kiyoung Choi](#), [Nikil D. Dutt](#)

January 2007 **Transactions on Design Automation of Electronic Systems** Issue 1

**Publisher:** ACM  [Request Permissions](#)

Full text available:  Pdf (1.48 MB) Additional Information: [full citation](#), [abstract](#), [references](#)




**Bibliometrics:** Downloads (6 Weeks): 4, Downloads (12 Months): 69, Citations: 1

Application-specific instructions can significantly improve the performance of code size of configurable processors. While generating new instructions and operation patterns has been a common way to improve performance, it is not always feasible.

**Keywords:** Application-specific instruction set processor (ASIP), ISA customization, specialization, bitwidth-economical, configurable processor, instruction set extension




#### 7 [Parallelizing load/stores on dual-bank memory embedded processor](#)

[Xiaotong Zhuang](#), [Santosh Pande](#)

- August 2006 **Transactions on Embedded Computing Systems (TECS)** ,  
 **Publisher:** ACM  [Request Permissions](#)  
 Full text available:  [Pdf](#) (746.64 KB) Additional Information: [full citation](#), [abstract](#), [ref](#)  
**Bibliometrics:** Downloads (6 Weeks): 4, Downloads (12 Months): 57, Citation

Many modern embedded processors such as DSPs support partitioned n X--Y memory or dual-bank memory) along with parallel load/store instr code density and performance. In order to effectively utilize the ...

**Keywords:** DSP architectures, memory bank allocation, parallel load/st optimization

- 8 [Java consistency: nonoperational characterizations for Java memory](#)  
 Alex Gontmakher, Assaf Schuster  
 November 2000 **Transactions on Computer Systems (TOCS)** , Volume 18 I  
**Publisher:** ACM  [Request Permissions](#)  
 Full text available:  [Pdf](#) (305.72 KB) Additional Information: [full citation](#), [abstract](#), [ref](#)  
**Bibliometrics:** Downloads (6 Weeks): 5, Downloads (12 Months): 29, Citation




The Java Language Specification (JLS) [Gosling et al. 1996] provides an the consistency of shared variables. The definition remains unchanged i currently under peer review, which relies on a specific abstract ...

**Keywords:** Java memory models, multithreading, nonoperational speci

- 9 [Co-synthesis of pipelined structures and instruction reordering const](#)  
 processors  
 Ing-Jer Huang  
 January 2001 **Transactions on Design Automation of Electronic Syste**  
 Issue 1  
**Publisher:** ACM  [Request Permissions](#)  
 Full text available:  [Pdf](#) (1.58 MB) Additional Information: [full citation](#), [abstract](#), [ref](#)  
**Bibliometrics:** Downloads (6 Weeks): 5, Downloads (12 Months): 28, Citation

This paper presents a hardware/software co-synthesis approach to pipe processor) design. The approach synthesizes the pipeline structure from architecture (behavioral) specification. In addition, it generates ...


**Keywords:** compiler instruction optimization\, instruction set processor taxonomy, synthesis

- 10 [Link-time compaction and optimization of ARM executables](#)  
 Bjorn De Sutter, Ludo Van Put, Dominique Charet, Bruno De Bus, Koen De  
 February 2007 **Transactions on Embedded Computing Systems (TECS)**  
**Publisher:** ACM  [Request Permissions](#)  
 Full text available:  [Pdf](#) (636.53 KB) Additional Information: [full citation](#), [abstract](#), [ref](#)  
**Bibliometrics:** Downloads (6 Weeks): 10, Downloads (12 Months): 112, Citati

The overhead in terms of code size, power consumption, and execution precompiled libraries and separate compilation is often unacceptable in where real-time constraints, battery life-time, and production ...

**Keywords:** Performance, compaction, linker, optimization

# 11 [Memory Ordering: A Value-Based Approach](#)

 [Harold W. Cain, Mikko H. Lipasti](#)

June 2004 **ISCA '04:** Proceedings of the 31st annual international sympos architecture

**Publisher:** ACM

Full text available:  [Pdf](#) (244.36 KB) Additional Information: [full citation](#), [abstract](#), [ref](#)

**Bibliometrics:** Downloads (6 Weeks): 1, Downloads (12 Months): 25, Citation

Conventional out-of-order processors employ a multi-ported, fully-associative guarantee correct memory reference order both within a single thread of threads in a multiprocessor system. As improvements in process technology

Also published in:


March 2004 **SIGARCH Computer Architecture News** Volume 32 Issue 2

# 12 [Fire-and-Forget: Load/Store Scheduling with No Store Queue at All](#)

[Samantika Subramaniam, Gabriel H. Loh](#)

December 2006 **MICRO 39:** Proceedings of the 39th Annual IEEE/ACM International Microarchitecture


**Publisher:** IEEE Computer Society

Full text available:  [Pdf](#) (357.14 KB) Additional Information: [full citation](#), [abstract](#), [ref](#)

**Bibliometrics:** Downloads (6 Weeks): 2, Downloads (12 Months): 32, Citation

Modern processors use CAM-based load and store queues (LQ/SQ) to support memory scheduling and store-to-load forwarding. However, the LQ and sizes required for large-window, high-ILP processors. Past research has

# 13 [Feedback-directed memory disambiguation through store distance analysis](#)

 [Changpeng Fang, Steve Carr, Soner Onder, Zhenlin Wang](#)

June 2006 **ICS '06:** Proceedings of the 20th annual international conference

**Publisher:** ACM [Request Permissions](#)


Full text available:  [Pdf](#) (696.61 KB) Additional Information: [full citation](#), [abstract](#), [ref](#)

**Bibliometrics:** Downloads (6 Weeks): 1, Downloads (12 Months): 25, Citation

Feedback-directed optimization has developed into an increasingly important optimizing compilers. Based upon profiling, memory distance analysis helps predicting data locality and memory dependences, and has seen ...

**Keywords:** memory disambiguation, store distance

# 14 [Bloom filtering cache misses for accurate data speculation and prefetching](#)

 [Jih-Kwon Peir, Shih-Chang Lai, Shih-Lien Lu, Jared Stark, Konrad Lai](#)

June 2002 **ICS '02**: Proceedings of the 16th international conference on S

**Publisher:** ACM  [Request Permissions](#)


Full text available:  Pdf (248.57 KB) Additional Information: [full citation](#), [abstract](#), [ref](#)

**Bibliometrics:** Downloads (6 Weeks): 3, Downloads (12 Months): 60, Citation

A processor must know a load instruction's latency to schedule the load the correct time. Unfortunately, modern processors do not know this lat dependent instructions should have been scheduled to ...


**Keywords:** bloom filter, data cache, data prefetching, data speculation

## 15 Toward kilo-instruction processors

 Adrián Cristal, Oliverio J. Santana, Mateo Valero, José F. Martínez

December 2004 **Transactions on Architecture and Code Optimization (**

**Publisher:** ACM  [Request Permissions](#)


Full text available:  Pdf (1.16 MB) Additional Information: [full citation](#), [abstract](#), [ref](#)

**Bibliometrics:** Downloads (6 Weeks): 3, Downloads (12 Months): 61, Citation

The continuously increasing gap between processor and memory speed: the performance achievable by future microprocessors. Currently, proce memory operations largely by maintaining a high number of ...

**Keywords:** Memory wall, instruction-level parallelism, kilo-instruction p multicheckpointing

## 16 Assembly instruction level reverse execution for debugging

 Tankut Akgul, Vincent J. Mooney III

April 2004 **Transactions on Software Engineering and Methodology (**

**Publisher:** ACM  [Request Permissions](#)


Full text available:  Pdf (1.18 MB) Additional Information: [full citation](#), [abstract](#), [ref](#)

**Bibliometrics:** Downloads (6 Weeks): 27, Downloads (12 Months): 72, Citatio

Assembly instruction level reverse execution provides a programmer wi program to a previous state in its execution history via execution of a "r ability to execute a program in reverse is advantageous for ...

**Keywords:** Debugging, reverse code generation, reverse execution

## 17 Early load address resolution via register tracking

 Michael Bekerman, Adi Yoaz, Freddy Gabbay, Stephan Jourdan, Maxim Kal

June 2000 **ISCA '00**: Proceedings of the 27th annual international sympos architecture

**Publisher:** ACM

Full text available:  Pdf (143.17 KB) Additional Information: [full citation](#), [abstract](#), [ref](#)

**Bibliometrics:** Downloads (6 Weeks): 2, Downloads (12 Months): 32, Citation

Higher microprocessor frequencies accentuate the performance cost of i

especially noticeable in the Intel's IA32 architecture where lack of register number of memory accesses. This paper presents novel, ...

Also published in:

May 2000 **SIGARCH Computer Architecture News** Volume 28 Issue 2

**18** [An efficient single-pass trace compression technique utilizing instructions](#)

 Aleksandar Milenković, Milena Milenković

January 2007 **Transactions on Modeling and Computer Simulation (TOMACS)**

**Publisher:** ACM  [Request Permissions](#)

Full text available:  Pdf (848.21 KB) Additional Information: [full citation](#), [abstract](#), [ref](#)

**Bibliometrics:** Downloads (6 Weeks): 8, Downloads (12 Months): 44, Citation

Trace-driven simulations have been widely used in computer architecture evaluations of new ideas and design prototypes. Efficient trace compression and decompression are crucial for contemporary workloads, as representative

**Keywords:** Instruction and data traces, instruction streams, trace compression

**19** [Load squared: adding logic close to memory to reduce the latency of load miss ratios](#)

 Sami Yehia, Jean-Francois Collard, Olivier Temam

June 2005 **MEDEA '04: Proceedings of the 2004 workshop on Memory Management Applications, systems and architecture**

**Publisher:** ACM

Full text available:  Pdf (287.96 KB) Additional Information: [full citation](#), [abstract](#), [ref](#)


**Bibliometrics:** Downloads (6 Weeks): 0, Downloads (12 Months): 16, Citation

Indirect memory accesses, where a load is fed by another load, are ubiquitous structures and sophisticated software conventions, such as the use of load-independent code. Unfortunately, they can be costly: ...

Also published in:

June 2005 **SIGARCH Computer Architecture News** Volume 33 Issue 3

**20** [The KScalar simulator](#)

 J. C. Mouré, Dolores I. Rexachs, Emilio Luque

March 2002 **Journal on Educational Resources in Computing (JERIC)**

**Publisher:** ACM  [Request Permissions](#)

Full text available:  Pdf (493.35 KB) Additional Information: [full citation](#), [abstract](#), [ref](#)





**Bibliometrics:** Downloads (6 Weeks): 11, Downloads (12 Months): 80, Citation

Modern processors increase their performance with complex microarchitectures, which makes them more and more difficult to understand and evaluate. KScalar is a tool that facilitates the study of such processors. It allows ...

**Keywords:** Education, pipelined processor simulator

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